PhD Proposal 2014

Title : Wideband ADC design for Power Amplifier Linearization

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Context :

With the increasing demand for connectivity with high communication rates, the mobile market and specially the smartphone market is growing exponentially. Mobile shipments are forecast to reach 2 billion in 2015 with a share of 75 % for smartphones [1]. Facing the explosive growth of mobile traffic, mobile operators are challenged with higher operational costs and potentially more disturbing CO_2 footprint in providing more capacity.In this context, one promising area for research concerns power amplifier technologies. An assessment of communications versatility and power efficiency shows that the power amplifier (PA) is the key component in the communications chain that could help achieve these objectives. Overcoming the trade-off Linearity/Efficiency inherent to PA's behavior is essential in order to reduce overall power consumption.

The proposed PhD work belongs to a NanoDesign project called LIFLEX (Linearization for Efficient and Flexible Future Mobile Networks).

The project LIFLEX aims at exploring new highly digital linearization techniques. We will propose the linearization of RF power amplifiers (PAs) using digital predistortion (DPD) technique. One of the most important constraints on DPD implementation is the digitization of PA output signal needed for the identification of PD model. The bandwidth of this signal may be 3 to 5 times wider than the bandwidth of the input signal. The sampling rate required for accurate compensation of out-of-band distortions is thus very high, and has a direct impact on power consumption and implementation complexity of DPD identification algorithms in the digital processor. The scientific approach is to innovate on the DPD digitization path, ADC architecture and identification algorithm, so that the whole is very advantageous in terms of complexity, speed of implementation convergence, and flexibility of use.

The supervising research team "Circuits and Communication Systems"(C2S), has its main axis of research in the field of cognitive radio and more specifically in the reconfigurable radio interface. Recently, the C2S team contributed to a European project CATRENE, PANAMA (power amplifiers and antennas for mobile applications). In this project, the work undertaken between C2S team and NXP concerned the measurement channel in digital predistortion loop. The research focuses on the ADC in the feedback loop.

Work content:

The ADC must be able to handle both a large dynamic range and a wide bandwidth because the measured signal spectrum covers a bandwidth thrice and five times the main signal band in order to digitize the third-order and fifth-order intermodulation products respectively. Components with such demanding specifications exist, like time interleaved pipeline ADC, but the power consumption is high and the performances are fixed without possible adjustment.

In this project, the scientific approach is to innovate at architecture level by designing new multi-path circuit architecture for ADC, based on the Bandpass Sigma Delta (SD). For a long time, the SD has been known for its accuracy and its low power consumption and now benefits from the new advanced CMOS technologies to reach both wide band and impressive Figure-of-Merit [2]. The aimed architecture is composed of a primary converter for the main signal which is the high power signal and secondary converters for adjacent bands which are low power signals. The concept of this new structure, adapted for multi-level signals, is original and is protected by a IMT- Telecom ParisTech patent [3]

The object of this PhD proposal is to continue the study to the point of a silicon implementation, as proof-point of the validity of the approach.

Tasks to be completed:

1. Bibliography study
2. Proposal of modifications of some basic analog cells in order to make possible the parallelization of CT BP SD modulators for versatile multi-band noise cancellation.
3. Synthesis and complete design of at least two modulators at schematic level, in respect to high performance specifications.
4. Defining the digital post-processing and synthesize the digital part.
5. Circuit Layout and Manufacturing
6. Circuit Evaluation and Valorization

Expected Results:

Simulation outstanding performances for bandwidth and accuracy equivalent to the state-of-the-art, but with reducing the **power consumption by 50% in comparison with classical architectures used for PA linearization.**

[1] N. DisplaySearch, "Smartphones to Pass 80% of Global Mobile Phone Shipments by 2017," Nov. 2013.[Online].Available:http://www.displaysearch.com/cps/rde/xchg/displaysearch/hs.xsl/131121_smartphones_to_pass_global_mobile_phone_shipments_by_2017.asp

[2] J. Harrison et al., Broadcom "**An LC Bandpass $\Delta\Sigma$ ADC with 70dB SNDR Over 20MHz Bandwidth Using CMOS DACs", 40 nm CMOS, 0,19 pJ/step, ISSCC 2012.**

[3] D.-K. G. Pham, P. Desgreys, P. Loumeau and T. Ridgers, "Method for Multiband Multilevel Analog-to-Digital Conversion", patent n° EG/VP-FR 12 53436, April 2012.